AMENDMENT TO THE CLAIMS

Please **AMEND** claim 1 as follows.

Please **CANCEL** claims 25-30 without prejudice or disclaimer.

A copy of all pending claims and a status of the claims is provided below.

1. (Currently Amended) A method of modifying circuit design source data of a three-dimensional structure for improving integrated circuit yield, the method being implemented with computer program code and hardware and comprising the steps of:

locating a problem structure using a shapes-processing tool; and

implementing at least one local modification to said three-dimensional structure to perform a fix-up process on the problem structure,

wherein the method comprises one of:

introduces jogs in wires of one layer arranged above wires of another layer;

introduces segments of wrong-way wiring in wires of one layer arranged above wires of another layer;

increases a space of minimum-spaced wires over a wider structure;

forms a dummy hole in an incompatible structure component of a first layer of the problem structure to reduce manufacturing defects of a structure component in a second layer of the problem structure; and

widens a trench of a lower layer of the problem structure under at least one wire of an upper layer of the problem structure.

2-4. (Canceled).

5. (Previously Presented) The method of claim 1, wherein the wider structure comprises an incompatible structure component of the problem structure.

6. (Previously Presented) The method of claim 1, wherein increasing a space of minimum-spaced wires comprises forming a dummy shape between the at least two wires and increasing the size of the dummy shape.

7. (Canceled).

8. (Previously Presented) The method of claim 1, wherein forming a dummy hole comprises forming a gap in the incompatible structure.

9 - 10. (Canceled).

11. (Previously Presented) A method of modifying circuit design source data for forming a multi-layer structure of a semiconductor device, comprising the steps of:

determining whether at least two minimum-spaced wires of an upper layer pass over a dishing-prone structure of a lower layer; and if so performing at least one of:

increasing a space between the two minimum-spaced wires of the upper layer in a region over the dishing-prone structure of the lower layer,

forming a dummy hole in a wide wire under the space between the two minimum-spaced wires; and

widening a trench between two wide wires under the space between the two minimum-spaced wires,

wherein the method is implemented with computer program code and hardware.

12. (Original) The method of claim 11, further comprising increasing the flexibility of at least one wire of the two minimum-spaced wires above the dishing-prone structure.

13. (Original) The method of claim 12, wherein increasing the flexibility of the at least one wire of the two minimum-spaced wires comprises forming at least one jog in the at least one wire.

14. (Original) The method of claim 11, wherein increasing a space between the two minimum-spaced wires comprises forming a dummy shape between the two wide wires by increasing the width of the dummy shape.

15. (Original) The method of claim 11, wherein forming the dummy hole in the wide wire comprises forming a gap configured to be filled with a dielectric in the wide wire approximately perpendicular to a long axis of the at least one wire of the two minimum-spaced wires.

16. (Original) The method of claim 11, further comprising causing a router to reroute at least one wire of the at least two minimum-spaced wires.

17. (Original) The method of claim 11, wherein widening the trench under the space between the two minimum-spaced wires comprises narrowing at least one wide wire of the two wide wires.

18. (Previously Presented) A method of modifying circuit design source data of a three-dimensional structure for forming a multi-layer structure of a semiconductor device, comprising the steps of:

forming a dishing-prone structure on a lower layer;

forming two minimum-spaced wires over the dishing-prone structure on an upper layer;

increasing a space between the two minimum-spaced wires in a region over the dishing-prone structure;

if the dishing-prone structure includes a wide wire, inserting a space for a dielectric island in the wide wire under at least one wire of the two minimum-spaced wires; and

if the dishing-prone structure includes a narrow trench between two wide wires, widening the narrow trench under of the space between the two minimum-spaced wires,

wherein the method is implemented with computer program code and hardware.

19. (Original) The method of claim 18, further comprising increasing the flexibility of at least one wire of the two minimum-spaced wires proximate the dishing-prone structure.

20. (Original) The method of claim 19, wherein increasing the flexibility of the at least one wire comprises forming at least one jog in the at least one wire of the two minimum-spaced wires.

21. (Original) The method of claim 18, wherein increasing a space between the two minimum-spaced wires comprises forming a dummy shape between the two minimum-spaced wires and increasing the width of the dummy shape.

22. (Original) The method of claim 18, wherein forming a dielectric island configured to be filled with a dielectric in the wide wire comprises forming a gap in the wide wire approximately perpendicular to a long axis of the at least one wire of the two minimum-spaced wires.

23. (Original) The method of claim 18, further comprising causing a router to reroute at least one wire of the at least two minimum-spaced wires.

24. (Original) The method of claim 18, wherein widening the narrow trench under at least one wire of the two minimum-spaced wires comprises narrowing at least one wide wire of the two wide wires.

25. – 30. (Canceled)

31. (Previously Presented) The method of claim 1, wherein the wider structure comprises a wider wire.

32. (Previously Presented) The method of claim 1, wherein the wider structure comprises a wider trench.

33. (Previously Presented) The method of claim 1, wherein the locating a problem structure using the shapes-processing tool comprises locating a problem structure remaining after post-layout optimizing using the shapes-processing tool.